42390.P12946

Amendment to Claim

1(Once amended). An apparatus, comprising:

a storage register to store first and second data values;

~~a channel to store data; and~~

~~a~~ first, second, third and fourth ~~terminal~~ data terminals to provide hexadecimal data from the ~~channel~~ data terminals in accordance with the first and second data values decoded to select four active terminals and the first, second and third terminals to provide octal data ~~from the channel~~ in accordance with the first and second data values decoded to select three active terminals~~.~~;

a terminal to provide a clock signal, wherein the hexadecimal data is changed with the clock signal; and

a terminal to provide a strobe signal, wherein an identity of ~~the channel~~ a register to output data is provided at the ~~first, second, third and fourth~~ appropriate data terminals during the strobe signal.

Please cancel claim 2.

3(Once amended). The apparatus of claim ~~2~~ 1 further comprising a terminal to receive a wait signal, wherein the hexadecimal data is not changed with the clock signal when the wait signal is received.

Please cancel claims 4 and 5.

6(Once amended). A device, comprising:

a storage register to store a data field value;

a ~~channel~~ second register to store data; ~~and~~

data terminals to provide data from the ~~channel~~ second register having a base value as determined by the data field value~~.~~;

a terminal to supply a strobe signal, wherein an identification value of a register to output data is provided on the data terminals during the strobe signal.

7(Original). The device of claim 6, wherein octal data is provided from the data terminals in accordance with the data field value.

8(Original). The device of claim 6, wherein hexadecimal data is provided from the data terminals in accordance with the data field value.

Please cancel claim 9.

10(Original). A system, comprising:

a first processor having a first set of terminals for outbound data and a second set of terminals for inbound data and including a register having a data field to determine the terminals in the first set that provide outbound data;

a Static Random Access Memory (SRAM) memory coupled to the first processor; and

a second processor having a first set of terminals for inbound data and coupled to the first set of terminals of the first processor, and a second set of terminals for outbound data and coupled to the second set of terminals of the first processor.

11(Original). The system of claim 10, further comprising a register in the second processor having a data field to determine the terminals in the second set that provide outbound data.

12(Original). The system of claim 10, further comprising a channel in the first processor to supply outbound data at the first set of terminals in a hexadecimal format in accordance with the data field.

13(Original). The system of claim 10, further comprising a channel in the first processor to receive inbound data at the second set of terminals in a hexadecimal format in accordance with the data field.

14(Original). The system of claim 10, further comprising a channel in the first processor to supply outbound data at the first set of terminals in an octal format in accordance with the data field.

15(Original). Th system of claim 10, further comprising a channel in the first processor to receive inbound data at the second set of terminals in an octal format in accordance with the data field.

16(Original). The system of claim 10 wherein the first processor is an applications processor.

17(Original). The system of claim 10 wherein the second processor is a baseband processor.

18(Once amended). A method, comprising:

writing a data bit of a data field;

storing data in a storage device; and

providing the stored data at data terminals in a first set of terminals, wherein a portion of the data terminals are inactive in accordance with a value of the data bit; and;

a terminal to provide a strobe signal, wherein an identity of a register to output data is provided at the data terminals during the strobe signal.

19(Original). The method of claim 18 comprising receiving data at data terminals in a second set of terminals, wherein a portion of the data terminals are inactive in accordance with a value of the data bit.

20(Original). The method of claim 18 further comprising providing a strobe signal in the first set of terminals, wherein the data terminals provide an identification of the storage device when the strobe signal is active.

21(Original). The method of claim 20, further comprising providing a clock signal in the first set of terminals, wherein the data terminals provide the stored data in a hexadecimal format in clock cycles of the clock signal that follow the strobe signal.

22(Original). The method of claim 20, further comprising providing a clock signal in the first set of terminals, wherein the data terminals provide the stored data in an octal format in clock cycles of the clock signal that follow the strobe signal.

23(Original). A method, comprising:

selecting data terminals from a group of data terminals to supply data;

supplying a clock signal from a first terminal;

supplying a strobe signal from a second terminal; and

providing data at the selected data terminals when the strobe signal is inactive, the data changing in accordance with the clock signal.

24(Original). The method of claim 23, further comprising providing a third terminal that receives a wait signal that keeps the data provided at the data terminals from changing.

25(Original). The method of claim 23, further comprising providing null data from the data terminals when a channel register that stores the data sent to the data terminals is empty.

26(Original). The method of claim 25, further comprising supplying an identification value corresponding to the channel register from the selected data terminals when the strobe signal is active.

27(Original). A method comprising:

transferring data from an applications processor to a baseband processor through a first set of data pins; and

transferring data from the baseband processor to the applications processor through a second set of data pins.

28(Original). The method of claim 27 further comprising programming a register in the applications processor to select data pins from the first set of data pins to provide hexadecimal, octal or binary data.

29(Original). The method of claim 27 further comprising programming a register in the baseband processor to select data pins from the second set of data pins to provide hexadecimal, octal or binary data.

30(Original). The method of claim 28 wherein transferring data from an applications processor to a baseband processor further comprises transferring a clock signal to the baseband processor.

31(Original). The method of claim 29 wherein transferring data from a baseband processor to an applications processor further comprises transferring a clock signal to the applications processor.

32(Original). An articl comprising a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

(a) transferring data from an applications processor to a baseband processor through a first set of data pins; and

(b) transferring data from the baseband processor to the applications processor through a second set of data pins.

33(Original). The article of claim 32, wherein the baseband processor includes a register, and wherein the instructions, when executed, further result in:

programming the register in the baseband processor to select data pins from the first set of data pins to provide hexadecimal, octal or binary data.

34(Original). The article of claim 32, wherein the applications processor includes a register, and wherein the instructions, when executed, further result in:

programming the register in the applications processor to select data pins from the second set of data pins to provide hexadecimal, octal or binary data.